## ABSTRACT

Disclosed herein is a synchronous SRAM-compatible memory using DRAM cells. In the synchronous SRAM-compatible memory of the present invention, a refresh operation is controlled in response to a refresh clock signal having a period "n" times a period of a reference clock signal. The refresh operation is performed while a chip enable signal /CS is inactivated. A writing/reading access operation is performed in response to a writing/reading command generated while the chip enable signal /CS is activated. Therefore, in the writing/reading access operation of the synchronous SRAM-compatible memory of the present invention, no delay of time occurs that would otherwise occur due to the refresh operation of the DRAM cells.